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(54) Title of the invention: Satellite digital broadcast receiver

(57) Abstract:
Problem to be solved: To attain the establishment of synchronization in a short time by setting the sweep starting frequency of a voltage controlled oscillator in asynchronous state near a frequency corresponding to data stored in a storing means.
Solution: When a microcomputer 8 detects a high level being the asynchronous state from a synchronization detection circuit 25 in a primary state such as at the time of supplying a power source or the time of changing a receiving frequency, digital data is given to a frequency synthesizer 20 so as to make a VCO 18 sweep by interruption processing. At this time, the output signal of a compactor 23 is ignored.

The range of frequencies to sweep is determined by considering the transponder of a satellite to be superimposed to a first IF signal, the deviation of the frequency of the local oscillator of a receiving antenna, a drift quantity. The frequency when the VCO 18 starts sweeping is set near the frequency corresponding to data held in a memory 24, that is data in which a set value to give the frequency synthesizer 20 at the time of AFC operation is periodically written.

[Claims]

[Claim 1]

The satellite broadcasting receiver for digital broadcasting including a voltage controlled oscillator that outputs signaling frequency for setting up received frequency, a synchronous detection means from which a synchronous state detects whether it is no in a demodulator circuit, a control means to which controls the mentioned above voltage controlled oscillator based on a detect output of the mentioned above synchronous detection means, a reference signal fixed to a fixed phase in a synchronous state is made to output, and a frequency sweep signal is made to output in an asynchronous state, a means to store data about oscillating frequency of the mentioned above voltage controlled oscillator in a synchronous state, the mentioned above control means sets up a sweep start frequency of the mentioned above voltage controlled

oscillator in an asynchronous state near the frequency corresponding to the mentioned above stored data.

[Claim 2] The satellite broadcasting receiver for digital broadcasting according to claim 1 with which oscillating frequency of a voltage controlled oscillator is controlled by a preset value to which a phase synchronization circuit is constituted including a frequency synthesizer, and a control means gives a voltage controlled oscillator to this frequency synthesizer.

[Claim 3] The satellite broadcasting receiver for digital broadcasting according to claim 2 with which a preset value given to a frequency synthesizer is stored by memory means, and a control means reads this stored value and gives a value of that neighborhood to a frequency synthesizer.

[Claim 4] The satellite broadcasting receiver for digital broadcasting according to claim 3 stored while a preset value given to a frequency synthesizer is periodically updated by memory means.

[Claim 5] The satellite broadcasting receiver for digital broadcasting according to claims 2 - 4 with which a means that carries out dividing of the frequency of the mentioned above voltage controlled oscillator is formed in a phase synchronization circuit and the division ratio is stored by memory means.

[Claim 6] The satellite broadcasting receiver for digital broadcasting according to claims 1 - 5 with which a control means sets up more narrowly than the sweep frequency range of 2nd next the 1st sweep frequency range according to a voltage controlled oscillator.

[Detailed description of the invention]

[0001]

[Field of the invention] Especially this invention relates to the receiver that has improved the frequency sweep method for performing an establishes synchronization about the satellite broadcasting receiver for digital broadcasting.

[0002]

[Description of the prior art] Although an AFC circuit (automatic frequency control circuit) is provided in the satellite broadcasting receiver for digital broadcasting and received frequency is generally held, unless a demodulator circuit will be in a synchronous state, in order that it may not operate, this AFC circuit needs to synchronize a demodulator circuit, even when there are the deviation and drift of frequency of the transponder of a satellite or a receiving antenna of a local transmitter. For this reason, for example, as shown on Institute of Television Engineers of Japan technical report Vol.17, Number 13, PP.13 - 18 (Feb.1993), in the asynchronous states at a power up or the time of received frequency change, the method that makes the

voltage-controlled oscillating frequency of a frequency changing circuit or a detector circuit sweep compulsorily in the fixed range and performs an establishes synchronization is proposed.
[0003] Drawing 6 is a block diagram showing an example of the conventional satellite reception system for digital broadcasting. If the signal by which digital modulation was carried out by MSK, QPSK, etc. is received by the RF section besides a drawing and the 1st IF signal is inputted into the female mold connector 1, it will be amplified with the amplifier 2 and will be changed into the 2nd IF signal by the mixer 3. In this mixer 3, the local signal generated by PLL (Phase Locked Loop) that consists of VCO (voltage controlled oscillator) 4, the loop filter 5, the frequency synthesizer 6, and the reference frequency oscillator 7 is used. The 2nd IF signal is distributed by the distributor 9 two times, turns into a baseband signal by the mixers 10 and 14 and the low pass filters 11 and 15, respectively, is used as digital data by A/D converters 12 and 16, and it is the original data with the QPSK/MSK demodulator 13.
[0004] Thus, in order to restore to the data by which digital modulation was carried out by MSK, QPSK, etc., there is the necessity (this is called carrier reproduction) of reproducing the reference signal fixed to the fixed phase.

Here, as the carrier reproduction method, the information on relative phase difference with a sending signal (carrier phase error signal) was extracted, and the method called the costas loop in which relative phase difference (carrier phase error) with a sending signal reproduces the reference signal of zero based on it is adopted. In a synchronous state, VCO 18 becomes a reference signal of a costas loop. In an asynchronous state, the analog multiplexer 39 chooses the input from the triangular wave generator 38 (frequency includes what is produced from 0.1 Hz at about 10 Hz by the source of an oscillation carrying out the A/D conversion and digital signal of an analog) in response to the output of the synchronization detection circuit 25, the frequency of VCO 18 is swept by inputting into the adder 22 with the carrier phase error signal acquired from the carrier phase error extracting circuit 26 and the loop filter 27 of a costas loop.

[0005] And if the oscillation of VCO 18 will enter in a capture range and will be in a synchronous state, the frequency of VCO 18 has a sweep stopped, when the output of the synchronization detection circuit 25 is reversed, and the analog multiplexer 39 chooses the input from the amplifier 37 and inputs into the adder 22 with a carrier phase error signal. The signal that amplified the carrier phase error signal with the amplifier 37 after passing the low pass filter 36 turns

into an AFC signal, and VCO 18 also performs AFC operation while operating so that a carrier phase error may become zero.

[0006]

[Problems to be solved by the invention] In this conventional satellite broadcasting receiver for digital broadcasting, in order to make a synchronization establish from an asynchronous state as soon as possible, the oscillating frequency of the triangular wave generator that controls a sweep must be raised, but the loop filter of a costas loop cannot be followed in that case, but when especially a receiving condition is bad (low C/N), it becomes difficult to establish the synchronization itself. Since time until it makes a synchronization establish will become long if it becomes impossible to synchronize a demodulator circuit with the deviation and drift of frequency of the transponder of a satellite or a receiving antenna and is too large, when the range of the frequency to sweep of a local oscillator is too narrow, it is necessary to limit to the proper range, thus to adjust the peak value. The purpose of this invention is to provide the satellite broadcasting receiver for digital broadcasting that can realize synchronization for a short time.

[0007]

[Means for solving the problem] A satellite broadcasting receiver for digital broadcasting of this invention, a voltage controlled oscillator that outputs

signaling frequency for setting up received frequency, a demodulator circuit controls the mentioned above voltage controlled oscillator based on a detect output of a synchronous detection means from which a synchronous state detects whether it is no, and the mentioned above synchronous detection means, including a control means to which a reference signal fixed to a fixed phase in a synchronous state is made to output, and a frequency sweep signal is made to output in an asynchronous state, this is equipped with a means to store data about oscillating frequency of a voltage controlled oscillator in a synchronous state and it functions as setting up a control means near the frequency corresponding to data that had a sweep start frequency of a voltage controlled oscillator in an asynchronous state stored.

[0008] Here, a phase synchronization circuit is constituted including a frequency synthesizer and a voltage controlled oscillator is considered as composition by which oscillating frequency of a voltage controlled oscillator is controlled by preset value which a control means gives to this frequency synthesizer. A preset value given to a frequency synthesizer is stored by memory means and a control means is considered as composition that reads this stored value and gives a value of that neighborhood to a frequency synthesizer. It stores, while a preset value given to a frequency synthesizer is periodically updated by memory means.

[0009]
[Embodiment of the invention] Next, an embodiment of the invention is described with reference to drawings. Drawing 1 is a block diagram showing one example of this invention. The female mold connector 1 is an input terminal of a tuner unit, and the electric wave (the 1st IF signal) changed into the 1st intermediate frequency by the low noise converter (LNC) of the receiving antenna besides a drawing is inputted by a coaxial cable. After the 1st IF signal is amplified with the amplifier 2, it is inputted into the mixer 3 and a down convert is carried out by being mixed with the signal of VCO 4 to the 2nd IF signal. VCO 4 constitutes PLL with the frequency synthesizer 6, the reference frequency oscillator 7, and the loop filter 5, and for every frequency which a receiver tends to receive with the digital signal of the microcomputer 8, oscillating frequency is determined and it is controlled.
[0010] On the other hand, after the mentioned above 2nd IF signal is distributed by the distributor 9, it is inputted into the mixer 10 and the mixer 14, respectively, and is mixed with the signal that distributed the signal of VCO 18 to 90 relative phase difference with the phase converter 17 90 degrees, respectively. The output of the mixer 10 and the mixer 14 passes, respectively, and the low pass filter 11 and the low pass filter 15 Later, it becomes a baseband signal, and it is changed into digital data by A/D

converter 12 and A/D converter 16, and becomes the original data with the QPSK/MSK demodulator 13.

[0011] Also a baseband signal is inputted into the carrier phase error extracting circuit 26 and a carrier phase error signal is acquired through the loop filter 27 of a costas loop. A carrier phase error signal is added with the output of the loop filter 19 by the adder 22 and serves as control voltage of VCO 18. VCO 18 constitutes PLL including this adder 22 with the frequency synthesizer 20, the reference frequency oscillator 21 and the adder 22, and oscillating frequency and a phase are controlled by the digital data that the microcomputer 8 gives to the frequency synthesizer 20.

[0012] It changes to frequency sweeps at the time of asynchronous, and the microcomputer 8 changes the digital data given to the frequency synthesizer 20 in response to the output of the synchronization detection circuit 25 of a demodulator circuit to AFC at the time of a synchronization. The digital data for AFC amplifies a carrier phase error signal with the comparator 23, and is generated based on the signal changed into the digital signal. The memory 24 may be for holding the digital data given to the frequency synthesizer 20 and volatility may be sufficient as it as long as it is provided with the nonvolatile or the power supply for backup.

[0013] Next, operation of the circuit of drawing 1 is explained. In the synchronization detection circuit 25, a «low» level is outputted in a synchronous state, and a demodulator circuit outputs a «high» level in an asynchronous state (the reverse of active may be sufficient) or that the microcomputer 8 looks at this output of the synchronization detection circuit 25, and a demodulator circuit is a synchronous state, it judges whether it is an asynchronous state and the output signal of the comparator 23 is read every 20 ms in a synchronous state, the case where the output signal of the comparator 23 is what amplified and digital signalized the carrier phase error signal, and the phase of VCO 18 is behind to the sending signal «high», a «low» level is outputted when you are following the level (active can become reverse).

[0014] When the output of the comparator 23 is a «high» level, the microcomputer 8, AFC operation is conversely performed by giving the digital data that 6.25 kHz of frequency of VCO 18 becomes high from the time of setting out last time to the frequency synthesizer 20, by giving digital data that becomes low 6.25 kHz from the time of setting out last time at the time of a «low» level. The oscillating frequency of VCO 18 is stored by writing in, while the microcomputer 8 updates the preset value given to the frequency synthesizer 20 to the memory 24 on a periodic target (for example, every 500 ms).

[0015] In the initial states at a power up or the time of received frequency change, if the microcomputer 8 detects the «high» level that is an asynchronous state from the synchronization detection circuit 25, as swept in VCO 18 by interrupt processing, digital data will be given to the frequency synthesizer 20. The output signal of the comparator 23 is disregarded at this time. The frequency range to sweep is decided in consideration of a deviation, a drift amount, etc. of frequency of the transponder of a satellite or the local oscillator of a receiving antenna on which the 1st IF signal is overlapped and in this example, 479.5 MHz that is the center frequency of the 2nd IF signal, VCO 18 is swept carrying out the step of every 6.25 kHz of the ranges of ±3 MHz for every mS a center. However, if the «low» level that is a synchronous state is detected from the synchronization detection circuit 25, it will be promptly stopped by sweep by interrupt processing, and will shift to the mentioned above AFC operation. The frequency in which VCO 18 starts a sweep is determined based on the data held at the memory 24, namely, the data that wrote in periodically the preset value given to the frequency synthesizer 20 at the time of AFC operation.
[0016] Drawing 2 shows the situation of the sweep by this embodiment. In this embodiment, frequency that separated 1 MHz from the data held at the memory 24 is made into a sweep start frequency, this is swept towards the data held at the memory 24, and a sweep of

the range up to -3 MHz described above at the maximum is considered as the 1st sweep. This is what depends the deviation of the local oscillation frequency of a satellite transponder or a receiving antenna on individual difference, it is what considered that it hardly changed in the short term and took only the short-term change factor into consideration also about the drift amount, in almost all cases, except for the case where a receiving condition is inferior, a demodulator circuit establishes a synchronization by the 1st sweep and in order to refer to frequency at the time of a synchronization last time moreover and to start a sweep, it synchronizes for a short time. When a demodulator circuit does not synchronize by the 1st sweep temporarily, it sweeps over the range of ±3 MHz next focusing on the center frequency of the 2nd IF signal.

[0017] Drawing 3 is a block diagram showing the example of composition of the mentioned above frequency synthesizer 20. The frequency synthesizer 20 includes the shift register 31, the data latch 30, the swallow counter 32, the programmable counter 33, the 2 modulus prescaler 35, the phase comparator 34, and the standard part cycle 40. The oscillating frequency fOSC of VCO 18 is given with a following formula.

$$fOSC=[(MxN)+A] \times fR / R$$

M: the dividing value of the smaller one of the dividing values of the 2 modulus prescaler 35
N: specification of programmable counter 33
A: the value of swallow counter 32
fR: the oscillating frequency of reference frequency oscillator 21
R: the preset value of standard counting-down circuit 40
[0018] According to this embodiment, the value of M 128, the value of fR 12.8 MHz, the value of R can be set to 4096 and the value of N can set up the values from 128 to 2047, and the value of A can set up the values from 0 to 127. The microcomputer 8 gives the binary value of A value and N value as serial data to the frequency synthesizer 20. A value and N value are changed into parallel data by the shift register 31, and are set as the swallow counter 32 or the programmable counter 33 through the data latch 30.
[0019] First, after counting A times what carried out 1 / 129 dividing of the fOSC by 2 modulus prescaler 35 at the swallow counter 32, 1-/(128 N+A) dividing of the fOSC is carried out by carrying out the time (N-A) count of what carried out 1 / 128 dividing of the fOSC by 2 modulus prescaler 35 by the programmable counter 33 shortly, by the voltage obtained by carrying out a phase comparison to the reference oscillation wave that carried out 1 / 40 dividing of the fR with the phase comparator 34, fOSC is controlled to oscillate by 3125 (128 N+A)Hz. Also A value «1» when it changes,

3.125 kHz of fOSC changes, namely, the icrocomputer 8 can set up the frequency of VCO 18 with the minimum step width of 3.125 kHz.

[0020] Also, in order to make a sweep start frequency into the frequency which separated 1 MHz from the data held at the memory 24, at the time of a sweep start, the data of the memory 24 to N «2» and A value «64» and the microcomputer 8 is made to calculate the increased value and what is necessary is just to set up the value to the frequency synthesizer 20

[0021] Drawing 4 is a drawing showing an example of the memory map of the memory 24 of this invention. Here, the microcomputer 8 divides the field that stores data in the memory 24 for every received frequency, so that the difference in the deviation of the local oscillation frequency for every transponder of a satellite can be disregarded. What is necessary is for the transponder of a satellite to be limited, and just to form the number of memory areas according to the specification, since the number of the transponders that receive changes with specifications of a satellite broadcasting receiver. Detection of the microcomputer 8 of that the synchronization detection circuit 25 is a «high» level will determine a sweep start frequency based on the data of the data area that agrees with the frequency that a receiver tends to receive.

[0022] Drawing 5 shows another embodiment about the frequency sweep method of this invention. If the time interval to which the step of the frequency is carried out is the same, since the way that narrows the frequency interval of a step can lower the cut off frequency of the loop filter 27 and equivalent noise bandwidth narrows, the carrier reproduction capability at the time of low C/N will increase. Then, if only the 1st sweep is made to sweep in ±1 MHz of the frequency stored by the memory 24 and a synchronization does not establish it temporarily in this embodiment there, carrying out the step of every 3.125 kHz for every mS, it is made to have swept in ±3 MHz focusing on the center frequency of the 2nd IF signal, carrying out the step of every 6.25 kHz for every mS next.

[0023]

[Effect of the invention] This invention is provided with a means to store the data about the oscillating frequency of the voltage controlled oscillator in a synchronous state as explained above, in order to set up the sweep start frequency of the voltage controlled oscillator in the asynchronous states at a power up, the time of received frequency change, etc. near the frequency corresponding to the data stored by this memory means and to perform a frequency sweep, it becomes possible to establish a synchronization for a short time.

In order to have a frequency synthesizer in the phase synchronization circuit including a voltage controlled

oscillator and to control the oscillating frequency of a voltage controlled oscillator by the preset value of this frequency synthesizer, it is effective in being able to set up arbitrarily the range of a frequency sweep and its step size, the adjustment becoming unnecessary and regulation of a sweep rate or the carrier reproduction capability at the time of low C/N is achieved.

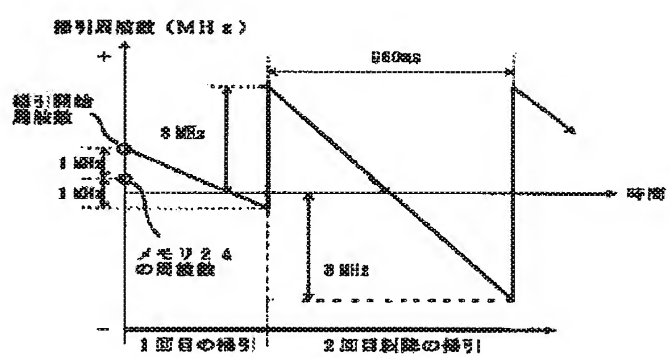
[Brief description of the drawings]

[Drawing 1] is a block diagram of one embodiment of the receiver of this invention.
[Drawing 2] is a time chart that shows a sweep of the frequency in the embodiment of drawing 1.
[Drawing 3] is a block diagram of the frequency synthesizer in the embodiment of drawing 1.
[Drawing 4] is a memory map drawing of the memory in this invention.
[Drawing 5] is a time chart that shows a sweep of the frequency in other embodiments of this invention.
[Drawing 6] is a block diagram of an example of the conventional receiver.

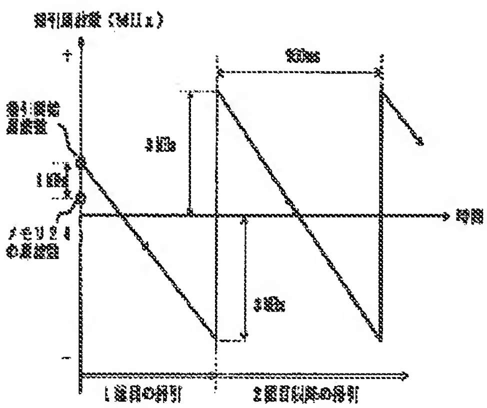
[Description of numerals]

3 Mixer
9 Distributor
10, 14 Mixer
13 QPSK/MSK demodulator
17 90 degree phase converter
18 VCO
20 Frequency synthesizer
21 Reference frequency oscillator
23 Comparator
24 Memory
25 Synchronization detection circuit
26 Carrier phase error extracting circuit
27 Loop filter

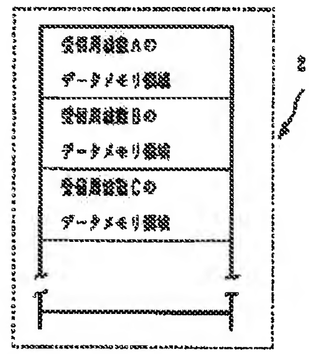
Drawing 5



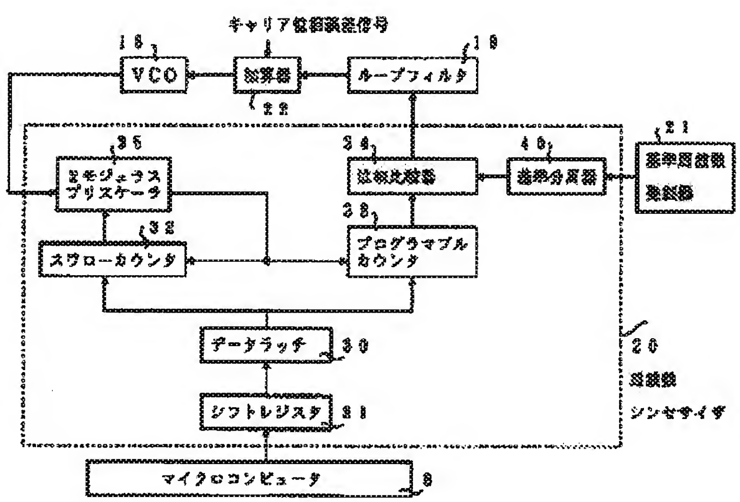
Drawing 2



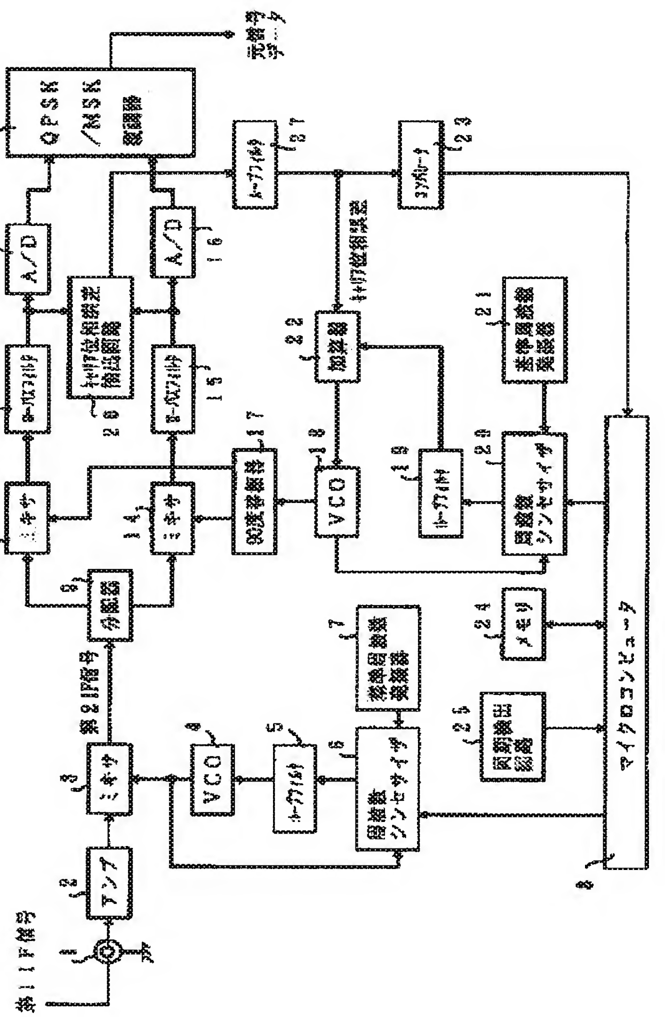
Drawing 4



Drawing 3



Drawing 1


QPSK
/MSK
復調器
A/D
A/D
VCO
VCO
ミキサ
ミキサ
ミキサ
アンプ
分配器
加算器
メモリ
マイクロコンピュータ

Drawing 6